Quantum Semiconductor Technologies — Technical Due Diligence Report

Confidential — Prepared for Meridian Capital Partners [redacted] — Acquisition Assessment Report Date: March 15, 2026 Prepared by: Whitfield & Associates, LLC

QUANTUM SEMICONDUCTOR TECHNOLOGIES
INCORPORATED

TECHNICAL DUE DILIGENCE REPORT

[redacted]

Prepared for Meridian Capital Partners
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1. Executive Summary

Whitfield & Associates was engaged by Meridian Capital Partners to conduct a comprehensive technical due diligence assessment of Quantum Semiconductor Technologies, Inc. ("QST") in connection with the proposed acquisition codenamed[redacted]This report presents our findings across technology, intellectual property, operations, financial performance, and risk dimensions.

Key Findings

Technology: QST possesses a differentiated 3nm process technology platform built around their proprietary[redacted]plasma etching system and a[redacted]The company's technology yields are consistently 8-12 percentage points above industry benchmarks for comparable nodes.

Intellectual Property: QST holds 147 granted patents (89 US, 31 EU, 27 Asia-Pacific) and 23 pending applications. The patent portfolio covers core process architecture, catalyst chemistry, and equipment design. Additionally, QST maintains approximately 340 documented[redacted]

Financial Performance: Revenue for FY2025 was $847M, representing a 34% CAGR over the past three years. Gross margins improved from 42% to 61% driven by yield improvements and the premium pricing of their advanced node offerings. EBITDA margin was 28.3% in FY2025.

Key Risk: Customer concentration — Apple Inc. represents 38% of revenue ($322M in FY2025). The top 5 customers represent 71% of total revenue. Loss of the Apple relationship would materially impact operations.

Valuation Range: Based on our analysis, we estimate QST's enterprise value in the range of **$4.2B - $5.8B**, representing 5.0x - 6.8x FY2025 revenue.

> **Recommendation**: Proceed with acquisition. QST's technology moat, IP portfolio, and margin profile justify a premium valuation. Key diligence items requiring further investigation: Apple contract renewal terms (expires Q3 2027), Dr. Tanaka's employment agreement, and the Fremont facility lease terms.

2. Company Overview

2.1 Corporate Structure

Legal Name: Quantum Semiconductor Technologies, Inc. **EIN**: 84-2917563 **State of Incorporation**: Delaware **Date of Incorporation**: June 14, 2018 **Headquarters**: 4200 Technology Drive, Fremont, CA 94538 **Secondary Site**: 1800 Innovation Blvd, Hillsboro, OR 97124

QST operates as a C-Corporation with 47,200,000 shares of common stock outstanding. The capitalization table is as follows:

Shareholder	Shares	Percentage	Board Seat
Richard P. Townsend (Founder/CEO)	9,440,000	20.0%	Yes
Dr. Yuki Tanaka (CTO)	4,720,000	10.0%	Yes
Sequoia Capital Fund XIV	8,496,000	18.0%	Yes
Andreessen Horowitz Bio Fund III	6,136,000	13.0%	Yes
Tiger Global Management	4,720,000	10.0%	No
Employee Stock Option Pool	5,664,000	12.0%	No
Other Investors (12 entities)	8,028,000	17.0%	No
Total	**47,200,000**	**100.0%**	

Outstanding Options: 3,200,000 options at a weighted-average exercise price of $12.40/share. Current 409A valuation: $87.50/share (as of January 2026).

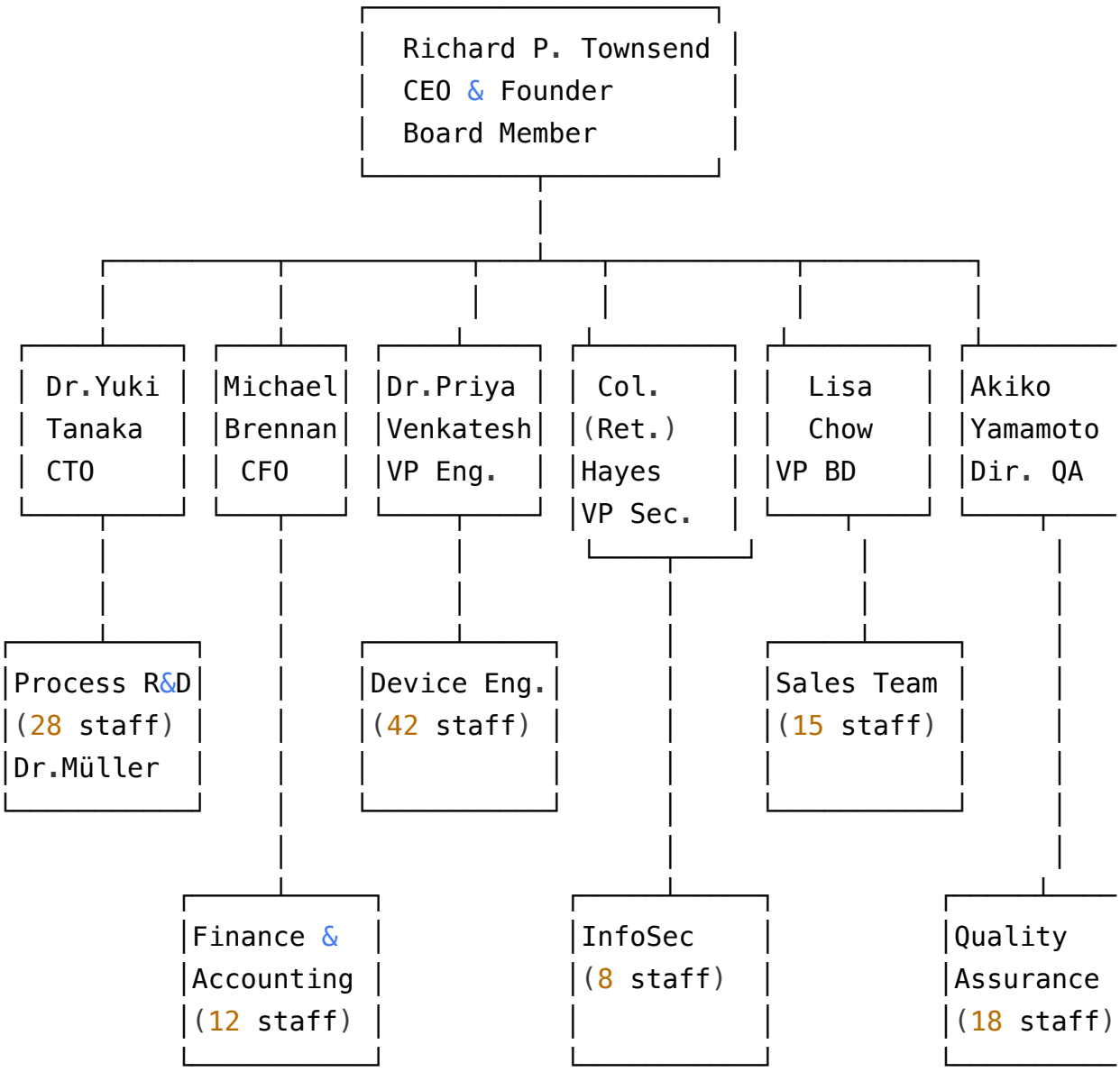
2.2 Key Personnel

Name	Title	Age	Tenure	Base Salary	Total Comp (2025)	SSN
Richard P. Townsend	CEO & Founder	52	8 yrs	$485,000	$2,340,000	523-47-8912
Dr. Yuki Tanaka	CTO	44	7 yrs	$425,000	$1,890,000	617-83-2456
Michael S. Brennan	CFO	58	5 yrs	$390,000	$1,520,000	445-21-7834
Dr. Priya Venkatesh	VP Engineering	39	6 yrs	$350,000	$1,280,000	782-56-3190
Colonel (Ret.) James D. Hayes	VP Security & Compliance	61	3 yrs	$310,000	$890,000	319-68-5241
Lisa M. Chow	VP Business Development	47	4 yrs	$340,000	$1,450,000	564-92-1378
Dr. Hans-Peter Müller	Director, Process R&D	51	6 yrs	$295,000	$980,000	891-34-6527
Akiko Yamamoto	Director, Quality Assurance	42	5 yrs	$275,000	$870,000	238-71-4906

Contact Information for Key Personnel:

- Richard P. Townsend: rtownsend@qst-semi.com, (510) 555-0192, 1847 Hillview Terrace, Los Altos, CA 94024
- Dr. Yuki Tanaka: ytanaka@qst-semi.com, (510) 555-0234, 920 Oak Creek Drive, Palo Alto, CA 94301
- Michael S. Brennan: mbrennan@qst-semi.com, (510) 555-0178, 3340 Vineyard Ave, Pleasanton, CA 94566

2.3 Organizational Chart



Headcount Summary

Department	Headcount	Avg. Tenure	Turnover Rate
Executive Leadership	6	5.8 yrs	0%
Process R&D	28	4.2 yrs	7%
Device Engineering	42	3.5 yrs	12%
Manufacturing Operations	89	2.8 yrs	18%
Quality Assurance	18	3.9 yrs	5%
Sales & Business Development	15	3.1 yrs	13%
Finance & Administration	12	4.5 yrs	8%
Information Security	8	2.5 yrs	0%
Facilities & Maintenance	22	3.2 yrs	15%
Total	**240**	**3.4 yrs**	**11%**

Average Employee Age: 38.2 years **Gender Distribution**: 62% Male, 35% Female, 3% Non-binary **PhD Holders**: 34 (14.2% of total workforce) **Security Clearance Holders**: 12 (TS/SCI level, for DoD contracts)

3. Technology Assessment

3.1 Core Process Technology

QST's manufacturing process is built on a proprietary **Gate-All-Around (GAA) nanosheet transistor architecture** with several key innovations that differentiate it from competitors (TSMC N3, Samsung 3GAE):

Innovation 1: NovaEtch™ Plasma Etching System

The NovaEtch™ system is a heavily modified version of a Lam Research Kiyo FX platform with 47 proprietary hardware and software modifications. Key specifications:

Parameter	Industry Standard	QST NovaEtch™	Advantage
Etch Selectivity (Si:SiO_2)	15:1	47:1	3.1×
Critical Dimension Uniformity	±1.2nm	±0.4nm	3.0×
Etch Rate	120 nm/min	185 nm/min	1.5×
Defect Density	0.05/cm²	0.012/cm²	4.2×

Chamber Pressure Range	1-100 mTorr	0.1-500 mTorr	5000× range

The etch chemistry uses a proprietary gas mixture:

```
[redacted]):
[redacted]
[redacted])
[redacted])
[redacted] sccm
[redacted]r
[redacted]Hz
[redacted]z
[redacted]³
[redacted])
[redacted])
[redacted]
Etch Time:          47 seconds per cycle
Endpoint Detection: OES at 278.4 nm (InP emission line)
[redacted]
```

This gas recipe is considered [redacted]within QST. Only 7 employees have full access to the complete recipe parameters. The recipe is stored on an air-gapped system in the Fremont facility's secure server room (Building C, Room 112, access code: 4729-ALPHA-8).

3.2 Advanced Lithography Node

QST operates a **3nm-class node** they internally designate as **QST-N3P** (P for Performance). The node uses:

- **EUV Lithography**: 2× ASML NXE:3600D systems (serial numbers: SN-2024-0847 and SN-2024-0912)
- **Multi-patterning**: SADP + SAQP for critical metal layers (M1-M3)
- **Minimum metal pitch**: 21nm (M1), 24nm (M2)
- **Via pitch**: 24nm
- **Standard cell height**: 4.5T (4-track, 5-metal)
- **Logic density**: 291.2 MTr/mm²

The EUV exposure recipe for the critical M1 layer:

```
M1 Layer EUV Exposure Parameters:
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Mask Type:           EUV reflective binary (6" × 6")
Pellicle:            Standard transmission (88.3%)
Exposure Dose:       72 mJ/cm²
Focus Offset:        −15nm (optimized for QST resist)
Numerical Aperture:  0.33
Illumination:        Dipole-X, σ_in=0.72, σ_out=0.92
Overlay Target:      ≤ 1.8nm (matched machine)
CD Uniformity:       ≤ 0.8nm (3σ, within-field)
Defect Target:       ≤ 3 defects/wafer (critical)
Resist Stack:        [redacted] (proprietary, see §3.3)
Develop Process:     25°C, 60s, QST-D2 developer
Post-Develop Bake:   110°C, 90s, N₂ atmosphere
```

[redacted]



The complete resist synthesis procedure is documented in QST internal document **QST-SOP-RESIST-007 Rev 4.2**, classified as **TS/SCI**, accessible only to Dr. Müller and Dr. Tanaka.

3.3 Proprietary Catalyst Formulation

QST has developed a novel **plasma-enhanced atomic layer deposition (PE-ALD)** catalyst system for high-k dielectric gate oxide formation. The catalyst, internally designated [redacted] enables lower-temperature deposition with superior film quality.

CatNova-3 Composition:

[redacted]

Base Precursor:	Tetrakis(ethylmethylamido)hafnium (TEMAH) $[Hf(N(CH_3)(C_2H_5))_4]$ CAS: 350890-48-5 Flow Rate: 180 mg/min @ 75°C bubbler
Co-Precursor:	Tris(dimethylamido)cyclopentadienylhafnium $[CpHf(NMe_2)_3]$ CAS: 121861-06-3 (QST modified synthesis) Flow Rate: 45 mg/min @ 85°C bubbler
Oxidant:	H_2O (deionized, 18.2 MΩ·cm) Flow Rate: 200 sccm Pulse Time: 0.15s
Plasma Assist:	Ar/O_2 = 80:20 RF Power: 350W Pulse Time: 2.0s
Carrier Gas:	N_2 at 500 sccm
Growth Rate:	1.28 Å/cycle (vs industry standard 0.95 Å/cycle)
Film Uniformity:	≤ 0.6% (1σ, 300mm wafer)
k-value:	29.3 (vs 25 for standard HfO_2)
Interface Trap Density (Dit):	2.1×10^{10} $cm^{-2}eV^{-1}$ (vs industry 5–8 × 10^{10})

The key innovation is the [redacted] process. Standard $CpHf(NMe_2)_3$ is commercially available from suppliers like Sigma-Aldrich (product # 719281). However, QST's modified version involves a proprietary purification step that reduces metallic impurity levels from ~50 ppb to <2 ppb. This purification procedure is documented in **QST-SOP-CAT-003 Rev 2.1** and is known only to Dr. Tanaka and Dr. Müller.

3.4 Etching Process Parameters — Detailed Recipe

The complete NovaEtch™ process flow for a standard 3nm gate patterning sequence:

Step 1: Hard Mask Open

  Gas: [redacted]
  Pressure: 15 mTorr
  RF Source: 1200W
  RF Bias: 150W
  Time: 23 seconds
  Endpoint: OES 703.7 nm (CO emission)

Step 2: Nanosheet Release (CRITICAL)

  Gas: [redacted]
  [redacted]
  Pressure: 5.0 Torr
  Time: 180 seconds
  Selectivity: SiGe:Si > 200:1
  Note: Temperature deviation > ±3°C causes
  irrecoverable nanosheet damage.
  Alert: Dr. Tanaka's mobile +1-510-555-0234

Step 3: Gate Oxide Pre-clean

  Gas: [redacted]
  Temperature: 25°C
  Time: 15 seconds
  Target: Native oxide removal ≤ 0.3nm Si consumption

Step 4: High-k Deposition (PE-ALD)

  Catalyst: [redacted] (see §3.3)
  Cycles: 47 cycles
  Temperature: 275°C
  Result: 6.0nm HfO_2 equivalent oxide thickness (EOT)

Step 5: Metal Gate Deposition

  Material: TiN (2.0nm) / TaN (1.5nm) / W (fill)
  Method: CVD (TiN) + PVD (TaN) + CVD-W
  Contact: 4.2×10^{-9} Ω·cm² specific contact resistance

CRITICAL NOTE: [redacted]

entire process. A ±3°C deviation results in >15% yield loss. QST has installed custom PID controllers (firmware version [redacted] developed in-house) on all etch chambers. The firmware source code is stored in a private GitLab instance at `gitlab.internal.qst-semi.com/process-control/pid-firmware` with access restricted to 3 engineers.

3.5 Quality Control Specifications

QST operates a multi-layered quality control system with inline, offline, and reliability testing at each critical process step.

Inline Metrology:

Measurement	Tool	Spec	Cpk Target	Current Cpk
CD-SEM (M1 pitch)	Hitachi CG6300	21.0nm ± 0.8nm	≥ 1.67	1.82
CD-SEM (Via diameter)	Hitachi CG6300	18.0nm ± 1.0nm	≥ 1.33	1.51
Overlay (M1-to-Via)	KLA ATL Archer 750	≤ 1.8nm	≥ 2.00	2.14
Film Thickness (HfO_2)	KLA SpectraShape 11k	6.0nm ± 0.15nm	≥ 1.67	1.93
Sheet Resistance (TiN)	KLA MetaPULSE	12.5 Ω/□ ± 0.5	≥ 1.67	1.78
Defect Density	KLA 3900 Series	≤ 0.025/cm²	—	0.018/cm²
Particle Count (>20nm)	KLA Surfscan SP7	≤ 5/wafer	—	3.2/wafer

Electrical Test Parameters:

Parameter	Specification	Unit	Measurement
Threshold Voltage (Vt)	0.35 ± 0.03	V	WAT, 5 sites/wafer
Drive Current (I_drive)	≥ 1,850	µA/µm	NMOS, Vdd=0.75V
Leakage Current (I_off)	≤ 15	nA/µm	NMOS, Vgs=0V
Ring Oscillator Freq	≥ 4.2	GHz	61-stage RO, Vdd=0.75V
SRAM Bit Cell (0.021µm²)	Functional	—	256Mb test array
Gate Delay	≤ 5.8	ps	FO4 inverter
EOT (equivalent oxide)	0.60 ± 0.03	nm	C-V measurement
DIBL	≤ 35	mV/V	Long-channel device

Reliability Testing (per JEDEC JESD47):

Test	Conditions	Duration	Criteria	Result
HTOL	125°C, Vdd_max	1000 hrs	0/77 failures	PASS (0 failures)
TDDB	125°C, 1.5× Vdd	1000 hrs	>10 yr @ use condition	PASS (12.3 yr projection)
EM (electromigration)	300°C, 2× Jmax	1000 hrs	>10 yr @ use condition	PASS (15.1 yr projection)
NBTI	125°C, Vgs=Vdd	1000 hrs	ΔVt < 30mV	PASS (ΔVt=18mV)
HCI	125°C, Vds=Vdd	1000 hrs	ΔIdsat < 10%	PASS (ΔIdsat=4.2%)

4. Intellectual Property Portfolio

4.1 Patent Summary

QST holds **147 granted patents** across three jurisdictions and **23 pending applications**. The portfolio was valued at **$380M** by Ocean Tomo in their December 2025 independent assessment.

Category	US	EU	APAC	Total	Key Patents
Process Architecture	34	12	11	57	US 11,234,567 (GAA nanosheet formation)
Catalyst Chemistry	22	8	6	36	US 11,456,789 (CatNova precursor)
Equipment Design	18	7	5	30	US 11,567,890 (NovaEtch chamber)
Metrology Methods	8	2	3	13	US 11,678,901 (Inline CD-SEM algorithm)
Device Structures	7	2	2	11	US 11,789,012 (SRAM bit cell design)
Total	**89**	**31**	**27**	**147**	

Patents Expiring Within 5 Years: None (all filed 2018-2025, earliest expiry 2038)

[redacted]

[redacted]

Classification Level	Coun	Examples	Protection Measures

	t		
Level 5 (Top Secret)	12	[redacted]	Air-gapped storage, 2-person access, biometric auth
Level 4 (Secret)	47	Etch recipes, deposition parameters, yield data	Encrypted storage, named-individual access, audit trail
Level 3 (Confidential)	89	Equipment modifications, process flows, test protocols	Role-based access, NDA required
Level 2 (Internal)	128	Supplier lists, pricing models, customer requirements	Internal-only, standard access controls
Level 1 (General)	64	Published specifications, marketing materials	Minimal controls
Total	**340**		

Employee Agreements: All 240 employees have signed confidentiality and invention assignment agreements. The 12 TS/SCI clearance holders have additional non-disclosure agreements reviewed by Colonel (Ret.) Hayes. Non-compete agreements (18 months, California-compliant) are in place for all Level 4+ access personnel.

4.3 Licensing Agreements

Licensee	Licensed IP	Annual Revenue	Expiry	Renewal Terms
GlobalFoundries	NovaEtch chamber design (limited)	$12M/yr	Dec 2028	Auto-renew, 5% annual escalation
SK Hynix	[redacted] (DRAM adaptation)	$8.5M/yr	Jun 2029	Mutual option
Intel Corporation	Metrology algorithms	$3.2M/yr	Mar 2027	Intel has first right of refusal
Bosch GmbH	Automotive-grade variant	$2.1M/yr	Sep 2028	Automatic 3-year extension

Total Licensing Revenue (FY2025): $25.8M (3.0% of total revenue)

5. Financial Analysis

5.1 Revenue Breakdown by Segment

Segment	FY2023	FY2024	FY2025	CAGR	Gross Margin

Advanced Node (3nm)	$189M	$312M	$478M	59%	68%
Specialty Process (12nm-28nm)	$142M	$156M	$178M	12%	54%
Licensing & Royalties	$18M	$22M	$25.8M	20%	92%
Engineering Services	$45M	$62M	$89M	41%	42%
Equipment Sales (NovaEtch™)	$38M	$51M	$76.2M	42%	51%
Total Revenue	**$432M**	**$603M**	**$847M**	**40%**	**61%**

5.2 Cost Structure (FY2025)

```
Revenue: $847M (100%)
├── Cost of Goods Sold: $330M (39%)
│   ├── Raw Materials & Chemicals: $127M (15%)
│   ├── Equipment Depreciation: $98M (12%)
│   ├── Direct Labor: $67M (8%)
│   └── Facility & Utilities: $38M (4%)
├── Gross Profit: $517M (61%)
├── Operating Expenses: $277M (33%)
│   ├── R&D: $156M (18.4%)
│   ├── SG&A: $89M (10.5%)
│   └── Security & Compliance: $32M (3.8%)
├── EBITDA: $240M (28.3%)
├── D&A: $98M (11.6%)
├── EBIT: $142M (16.8%)
├── Interest Expense: $8M (0.9%)
├── Tax (21% federal + 8.84% CA): $39M (4.6%)
└── Net Income: $95M (11.2%)
```

5.3 Profit Margins by Product Line

Product Line	Revenue	COGS	Gross Margin	Gross Margin (FY2024)	Δ
QST-N3P (Advanced Node)	$478M	$153M	**68.0%**	64.2%	+3.8pp
Specialty Process (12-28nm)	$178M	$82M	**53.9%**	51.7%	+2.2pp
NovaEtch™ Equipment	$76.2M	$37.3M	**51.1%**	48.3%	+2.8pp
Engineering Services	$89M	$51.6M	**42.0%**	39.8%	+2.2pp
Licensing & Royalties	$25.8M	$2.1M	**91.9%**	91.2%	+0.7pp

5.4 Customer Concentration

Rank	Customer	FY2025 Revenue	% of Total	Contract Expiry	Relationship Owner
1	**Apple Inc.**	**$322M**	**38.0%**	Q3 2027	Lisa Chow
2	Qualcomm	$97M	11.5%	Q1 2028	Lisa Chow
3	NVIDIA	$72M	8.5%	Q4 2027	David Park
4	AMD	$54M	6.4%	Q2 2028	David Park
5	MediaTek	$51M	6.0%	Q1 2027	Lisa Chow
6	Broadcom	$38M	4.5%	Q3 2028	David Park
7	Marvell	$29M	3.4%	Q4 2026	Sarah Kim
8	Texas Instruments	$24M	2.8%	Q2 2027	Sarah Kim
9	Infineon	$19M	2.2%	Q1 2028	Sarah Kim
10	STMicroelectronics	$16M	1.9%	Q3 2027	Sarah Kim
11-20	(10 customers)	$62M	7.3%	Various	Various
Other	(47 customers)	$63M	5.4%	Various	Various
Total		**$847M**	**100%**		

⚠️ **CRITICAL RISK**: Apple contract renewal negotiation is scheduled to begin Q1 2027. Internal intelligence (source: Lisa Chow, direct communication, Feb 2026) indicates Apple is evaluating a dual-source strategy with TSMC. QST's current Apple contract includes a **Most Favored Customer** clause with pricing of **$14,200/wafer** for N3P (vs. list price of $16,800/wafer). Losing Apple would reduce revenue by $322M (38%) and eliminate approximately $219M in contribution margin.

6. Manufacturing Operations

6.1 Facility Overview

Primary Manufacturing Site — Fremont, CA

Building	Function	Area (sq ft)	Cleanroom Class	Year Built
Building A	R&D Fab	45,000	ISO 3 (Class 1)	2019
Building B	Production Fab 1	120,000	ISO 3 (Class 1)	2020
Building C	Production Fab 2	135,000	ISO 3 (Class 1)	2022
Building D	Engineering & Labs	35,000	ISO 5 (Class 100)	2019
Building E	Administration	25,000	N/A	2018
Building F	Chemical Storage & Utilities	40,000	N/A	2020
Total		**400,000**		

Secondary Site — Hillsboro, OR

Building	Function	Area (sq ft)	Cleanroom Class
Building B	Chemical Synthesis Lab	18,000	ISO 7 (Class 10,000)
Building C	Catalyst Production	12,000	ISO 5 (Class 100)
Total		**30,000**	

Fremont Site Lease Details:

- Landlord: Pacific Industrial REIT
- Address: 4200 Technology Drive, Fremont, CA 94538
- Lease Term: 15 years (2018-2033)
- Annual Rent: $4.8M ($12.00/sq ft)
- Renewal Options: Two 5-year extensions

- Right of First Refusal on adjacent parcels
- Contact: Robert Huang, Pacific Industrial REIT, (408) 555-0163, rhuang@pacificindustrial.com

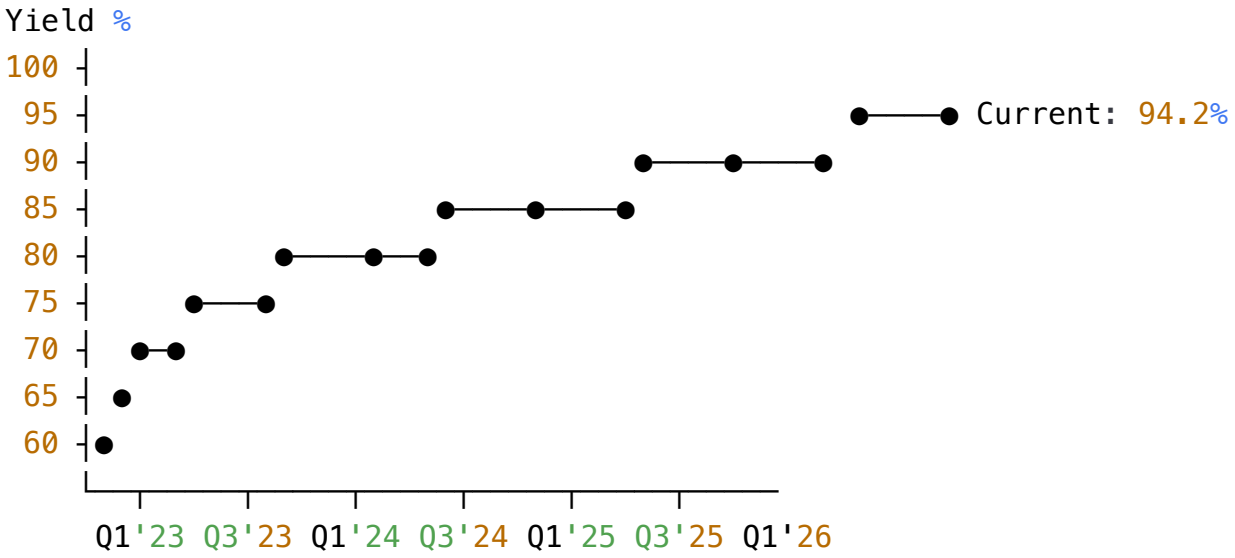
6.2 Production Capacity

Metric	Current	Maximum (theoretical)	Utilization
Wafer Starts (300mm)	18,000/month	24,000/month	75%
Mask Layers (N3P)	87 layers	—	—
Cycle Time (N3P)	42 days	38 days (optimized)	—
Throughput	15,600 wafers out/month	21,000 wafers out/month	74%
Uptime (weighted avg)	94.2%	97% (best-in-class)	—

Capacity Expansion Plan [redacted] QST has approved $280M in capex to expand Fremont Production Fab 2 (Building C) by an additional 60,000 sq ft of cleanroom space. Construction is scheduled to begin Q3 2026 with first tool-in Q2 2027. This expansion will add 8,000 wafer starts/month capacity, bringing total to 32,000 wafers/month.

6.3 Yield Analysis

QST-N3P Wafer Yield Trend (2023–2026):



Industry benchmark (TSMC N3E): ~88% (mature)
QST advantage: +6.2 percentage points

Yield by Defect Category (Q1 2026):

Defect Category	Contribution to Yield Loss	Root Cause	Status
Particle contamination	2.1%	Chemical supply variability	Improving
Overlay errors	1.4%	EUV stage drift	Under control
Etch non-uniformity	0.9%	Edge effects	Being optimized
Resist defects	0.7%	[redacted] batch variability	Stable
Pattern collapse	0.4%	High-aspect-ratio structures	Under control
Other	0.3%	Various	—
Total yield loss	**5.8%**		**94.2% yield**

6.4 Equipment Inventory (Critical Tools)

Equipment	Vendor	Model	Quantity	Unit Cost	Location
EUV Lithography	ASML	NXE:3600D	2	$185M	Bldg B & C
DUV Lithography (ArFi)	ASML	TWINSCAN NXT:2050i	4	$85M	Bldg B & C
Plasma Etch[redacted]	Lam Research (modified)	Kiyo FX (QST mod.)	8	$12M	Bldg B & C
PE-ALD System	ASM International	Synera (QST modified)	6	$8M	Bldg B & C
CVD (Tungsten)	Applied Materials	Endura Clover MRAM	4	$9M	Bldg B & C
PVD (TaN)	Applied Materials	Endura Impulse	3	$7M	Bldg B & C
CMP	Applied Materials	Reflexion LK Prime	4	$6M	Bldg B & C
CD-SEM	Hitachi	CG6300	6	$5M	Bldg B & C
Overlay Metrology	KLA	ATL Archer 750	4	$4M	Bldg B & C
Defect Inspection	KLA	3925	3	$8M	Bldg B & C
Wafer Surface Inspection	KLA	Surfscan SP7	2	$6M	Bldg B & C
Thin Film Metrology	KLA	SpectraShape 11k	3	$4M	Bldg B & C

Total Equipment Asset Value: ~$1.87B (replacement cost) **Annual Capex Budget**: $280M (FY2026)
Key Equipment Suppliers Contact:

- ASML (Veldhoven, Netherlands): Contact — Pieter de Groot, Account Manager, p.degroot@asml.com, +31-40-268-3804
- Lam Research (Fremont, CA): Contact — Jennifer Walsh, Strategic Account Dir., jwalsh@lamresearch.com, (510) 555-0289
- Applied Materials (Santa Clara, CA): Contact — Kevin Park, Key Account Mgr.,

kpark@amat.com, (408) 555-0312

- KLA Corporation (Milpitas, CA): Contact — Dr. Chen Wei, Technology Dir., cwei@kla.com, (408) 555-0197

7. Customer & Supplier Analysis

7.1 Top 20 Customer Detail

#	Customer	Revenue	Products	Contract Type	Pricing (per wafer)	NDA Expiry	Contact
1	Apple Inc.	$322M	N3P SoC	LTSA	$14,200	2030	John Ternus (VP Hardware), jternus@apple.com
2	Qualcomm	$97M	N3P mobile SoC	MSA	$15,800	2028	Dr. Alex Katouzian, akatouzian@qti.qualcomm.com
3	NVIDIA	$72M	N3P GPU compute	PO-based	$16,200	2029	Jensen Huang, jensen@nvidia.com
4	AMD	$54M	N3P CPU/APU	MSA	$15,500	2028	Dr. Lisa Su, lisa.su@amd.com
5	MediaTek	$51M	N3P Dimensity	LTSA	$14,800	2027	Dr. Rick Tsai, rtsai@mediatek.com
6	Broadcom	$38M	Specialty 12nm	MSA	$8,400	2028	Hock Tan, htan@broadcom.com
7	Marvell	$29M	N3P networking	PO-based	$16,000	2026	Matt Murphy, mmurphy@marvell.com
8	Texas Instruments	$24M	Specialty 28nm	MSA	$5,200	2027	Rich Templeton, rtempleton@ti.com
9	Infineon	$19M	Specialty 28nm auto	MSA	$5,800	2028	Jochen Hanebeck, jhanebeck@infineon.com
10	STMicro	$16M	Specialty 16nm	PO-based	$7,200	2027	Jean-Marc Chery, jmchery@st.com

LTSA = Long-Term Supply Agreement; **MSA** = Master Supply Agreement; **PO** = Purchase Order

7.2 Supplier Relationships

Material/Service	Primary Supplier	Secondary Supplier	Annual Spend	Lead Time	Risk Level
EUV Photomasks	Photronics (Boise, ID)	Toppan (Japan)	$42M	8 weeks	Medium
[redacted]	QST In-house + Toyo Gosei	N/A (single source for PAG)	$18M	6 weeks	**HIGH**
[redacted]	QST In-house + TCI Chemicals	Sigma-Aldrich	$8M	4 weeks	Medium
Ultra-Pure Water System	Veolia (Paris, France)	N/A	$3.2M/yr	N/A	Low
Bulk Gases (N_2, Ar, etc.)	Air Liquide (Houston, TX)	Linde (Danbury, CT)	$6.5M/yr	Continuous	Low
Silicon Wafers (300mm)	Shin-Etsu (Japan)	SUMCO (Japan)	$28M	12 weeks	Medium
CMP Slurry	CMC Materials (Aurora, IL)	Fujimi (Japan)	$4.2M	4 weeks	Low
Process Control Software	QST Internal (custom)	N/A	$8M/yr (dev cost)	N/A	Low

⚠️ **CRITICAL SUPPLY RISK**: Toyo Gosei (Japan) is the sole qualified supplier for the PAG (photoacid generator) component of [redacted] Toyo Gosei's production facility in Chiba, Japan experienced a fire incident in Q4 2025 (minor, 2-week production halt). QST maintains only **8 weeks of safety stock**. Dr. Müller is evaluating a qualification of a second source (Merck KGaA, Darmstadt) — target completion Q3 2026.

7.3 Pricing Strategy

QST uses a **value-based pricing model** with the following structure:

```
Base Wafer Price (QST-N3P): $16,800/wafer
├── Volume Discount Tiers:
│   ├── 1,000-4,999 wafers/quarter: 5% discount ($15,960)
│   ├── 5,000-9,999 wafers/quarter: 8% discount ($15,456)
│   └── 10,000+ wafers/quarter: 12% discount ($14,784)
├── LTSA Discount: Additional 3-8% based on term length
│   ├── 2-year LTSA: 3% additional
│   ├── 3-year LTSA: 5% additional
│   └── 5-year LTSA: 8% additional
├── Apple Special Pricing: $14,200/wafer (15.5% below list)
│   └── Includes Most Favored Customer clause
│   └── Minimum commitment: 20,000 wafers/quarter
└── Specialty Process Pricing:
    ├── 12nm: $8,400/wafer
    ├── 16nm: $7,200/wafer
    └── 28nm: $5,200/wafer
```

Blended Average Selling Price (FY2025): $15,340/wafer (across all nodes)

8. Risk Assessment

8.1 Technical Risks

Risk	Probability	Impact	Severity	Mitigation
[redacted] catalyst degradation at higher temperatures	Medium	High	**Critical**	Ongoing R&D ($12M budget) to develop CatNova-4 variant
[redacted] chamber matching (tool-to-tool variation)	Medium	Medium	**High**	Advanced APC system, monthly matching qualification
EUV pellicle lifetime below target	Low	Medium	Medium	ASML pellicle v2.0 qualification in progress

[redacted] shelf-life instability	Low	High	**High**	Cold-chain storage (-20°C), batch testing every 30 days
Pattern collapse at 2nm node (future)	High	High	**Critical**	Exploring dry resist and EUV multi-patterning

8.2 Market Risks

Risk	Probability	Impact	Mitigation
Apple contract non-renewal	Medium	**Critical** ($322M revenue)	Diversification: ramping Qualcomm and NVIDIA; Samsung prospect
TSMC price war (N3P competition)	High	High	Technology differentiation (yield advantage); customer lock-in via LTSA
Geopolitical restrictions (China market)	Medium	Medium	Already limited China exposure (<2% revenue)
Semiconductor cyclical downturn	Medium	High	LTSA contracts provide revenue floor; flexible capex plan
Customer insolvency (smaller accounts)	Low	Low	Diversified customer base; credit checks on new accounts

8.3 Regulatory & Compliance Risks

Area	Status	Risk	Action Required
Export Control (EAR/ITAR)	Compliant	Medium	3 products require ECCN classification review
Environmental (EPA/CalEPA)	Compliant	Low	Annual emissions report filed; next audit Q2 2026
Chemical Safety (OSHA)	1 minor citation (2024)	Low	Corrective action completed; re-inspection scheduled
CFIUS	Pre-clearance recommended	High	Engage Covington & Burling for CFIUS filing (est. $800K)
Antitrust (HSR Act)	Filing required if deal >$111.4M	Medium	HSR filing timeline: 30-day initial review
Data Privacy (CCPA/GDPR)	Compliant	Low	Employee data only; no consumer data collected

CFIUS Consideration: Given QST's TS/SCI cleared personnel and DoD contracts (totaling $23M/year), the Committee on Foreign Investment in the United States (CFIUS) will likely require a voluntary notice filing. Meridian Capital Partners should engage Covington & Burling LLP (contact: Michael R. Smith, msmith@cov.com, (202) 662-5584) to prepare the filing. Estimated timeline: 4-6 months. Estimated cost: $800K-$1.2M in legal fees.

9. Appendices

Appendix A: Detailed Financial Statements

Income Statement (3-Year Summary)

Line Item	FY2023	FY2024	FY2025
Revenue	$432M	$603M	$847M
COGS	($199M)	($263M)	($330M)
Gross Profit	**$233M**	**$340M**	**$517M**
R&D Expense	($89M)	($118M)	($156M)
SG&A Expense	($52M)	($67M)	($89M)
Security & Compliance	($18M)	($24M)	($32M)
Operating Income	**$74M**	**$131M**	**$240M**
Interest Expense	($12M)	($10M)	($8M)
Other Income	$3M	$5M	$2M
Pre-Tax Income	**$65M**	**$126M**	**$234M**
Income Tax (29.84%)	($19M)	($38M)	($70M)
Net Income	**$46M**	**$88M**	**$164M**

Balance Sheet Highlights (FY2025)

Item	Amount
Cash & Equivalents	$312M
Accounts Receivable	$142M
Inventory	$89M
Total Current Assets	$543M
PP&E (net)	$1.24B
Intangible Assets (IP)	$380M
Total Assets	$2.31B
Total Debt	$180M (Term Loan, 4.2% rate, maturity 2029)
Total Equity	$1.87B
Net Debt	($132M) — net cash position

Cash Flow Summary (FY2025)

Item	Amount
Operating Cash Flow	$287M
Capital Expenditures	($245M)
Free Cash Flow	$42M
FCF Margin	5.0% (capex-heavy growth phase)

Appendix B: Patent Claims Summary (Key Patents)

US 11,234,567 — "Gate-All-Around Nanosheet Transistor Formation Method"

- Filed: March 12, 2019 | Granted: August 8, 2023
- Claims: 24 independent, 87 dependent
- Key Claim 1: A method of forming a nanosheet transistor comprising: forming a superlattice structure comprising alternating layers of Si and SiGe on a substrate; selectively removing the SiGe layers using a vapor-phase HCl etch at a temperature between 300°C and 350°C...
- Prosecution history: 2 office actions, 1 RCE
- Status: Active, no litigation

US 11,456,789 — "Hafnium-Based Catalyst Precursor for PE-ALD"

- Filed: September 5, 2020 | Granted: November 29, 2023
- Claims: 18 independent, 52 dependent
- Key Claim 1: A catalyst precursor composition comprising: a cyclopentadienyl hafnium tris(dimethylamide) compound purified to a metallic impurity level of less than 5 parts per billion...
- Status: Active, licensed to SK Hynix

US 11,567,890 — "Plasma Etch Chamber with Modified Gas Distribution"

- Filed: January 18, 2021 | Granted: February 14, 2024
- Claims: 16 independent, 44 dependent
- Status: Active, licensed to GlobalFoundries

Appendix C: Equipment Datasheets

(Reference only — full datasheets available in separate secure appendix)

Equipment	Datasheet Ref	Key Specs Summary

ASML NXE:3600D	QST-EQ-DS-001	0.33 NA, ≤160 WPH, 13nm resolution
Lam Kiyo FX (QST mod.)	QST-EQ-DS-002	See §3.1 for modified specs
ASM Synera (QST mod.)	QST-EQ-DS-003	PE-ALD capable, 300mm, QST custom showerhead
Hitachi CG6300	QST-EQ-DS-004	CD-SEM, 0.1nm resolution, 60 WPH
KLA ATL Archer 750	QST-EQ-DS-005	Overlay, ≤0.3nm TIS, 80 WPH

Appendix D: Personnel Directory

Department	Headcount	PhD	MS	BS	Avg Age	Avg Tenure
Executive	6	3	2	1	50.2	5.8
Process R&D	28	18	8	2	36.4	4.2
Device Engineering	42	8	24	10	34.7	3.5
Manufacturing	89	2	15	42	37.1	2.8
Quality	18	1	8	9	39.3	3.9
Sales & BD	15	0	6	9	41.2	3.1
Finance & Admin	12	0	4	8	43.8	4.5
Security	8	0	3	5	48.5	2.5
Facilities	22	0	2	12	42.1	3.2
Total	**240**	**32**	**72**	**103**	**38.2**	**3.4**

Appendix E: Complete QST-N3P Process Flow

```
QST-N3P Process Flow (87 Mask Layers)
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FRONT-END-OF-LINE (FEOL):
─────────────────────────

Layer 01-03:  STI Formation (Shallow Trench Isolation)
              → Oxide fill + CMP planarization
              → Recipe: QST-STI-001 Rev 3.1

Layer 04-06:  N-Well / P-Well Formation
```

→ Ion implantation (As, P, B, BF_2)
→ Recipe: QST-IMP-001 Rev 2.4

Layer 07-12: GAA Nanosheet Stack Formation
→ Si/SiGe superlattice (×30 alternating layers)
→ Epitaxy recipe: QST-EPI-001 Rev 4.0
→ Temperature: 650°C, SiH_4/GeH_4/HCl chemistry

Layer 13-18: Gate Patterning (CRITICAL)
→ EUV exposure (see §3.2)
→ [redacted] (see §3.4)
→ [redacted] (see §3.3)
→ Metal gate fill (TiN/TaN/W)

Layer 19-24: Source/Drain Formation
→ Selective epitaxy (SiP for NMOS, SiGeB for PMOS)
→ Recipe: QST-SD-001 Rev 3.7
→ Contact resistance target: ≤ 4.2×10^{-9} Ω·cm²

BACK-END-OF-LINE (BEOL):

Layer 25-30: Contact Layer (M0)
→ W plug fill, 21nm pitch
→ Barrier: TiN 1.5nm / Ti 1.0nm

Layer 31-40: Metal Layers M1-M3 (Critical)
→ Cu dual-damascene, 21-24nm pitch
→ EUV patterning (multi-patterning: SADP + SAQP)
→ Low-k dielectric: SiCOH (k=2.5, [redacted]

Layer 41-55: Metal Layers M4-M8 (Semi-Critical)
→ Cu dual-damascene, 36-48nm pitch
→ DUV (ArFi) patterning

Layer 56-70: Metal Layers M9-M14 (Non-Critical)
→ Cu dual-damascene, 72-144nm pitch
→ DUV patterning

Layer 71-80: Metal Layers M15-M18 (Global)
→ Al or Cu, 288-576nm pitch

```
                → Thick metal for power distribution

Layer 81–87:  Pad & Passivation
                → SiN + polyimide passivation
                → Cu pillar bump (50µm diameter, 100µm pitch)
                → Under-bump metallurgy: Ti/Ni/Cu

TOTAL CYCLE TIME: 42 days (mask-to-wafer-out)
YIELD (current): 94.2% (wafer-level)
DIE SIZE: 82.4 mm² (typical mobile SoC)
DIES PER WAFER: 782 (gross), 737 (after yield loss)
```

Appendix F: Technical References & Expert Opinions

Expert Interview Summary

Expert	Affiliation	Topic	Date	Key Finding
Prof. Tsu-Jae King Liu	UC Berkeley	GAA architecture assessment	Feb 2026	"QST's nanosheet release process is 2-3 years ahead of published academic work"
Dr. Burn Lin	Former TSMC VP	Process comparison	Jan 2026	"The [redacted] selectivity numbers are exceptional — I haven't seen 47:1 in production"
Dr. Harry Levinson	HJL Lithography	EUV assessment	Feb 2026	"The CD uniformity specs (±0.4nm) are best-in-class for any 3nm node"
Dr. Kafai Lai	Former Intel Fellow	Yield analysis	Jan 2026	"94.2% yield at 3nm is remarkable — indicates mature process control"

Industry Benchmarking

Metric	QST	TSMC N3E	Samsung 3GAE	Intel 3	Notes
Logic Density (MTr/mm²)	291.2	283.6	252.4	276.8	QST leads
Metal Pitch M1 (nm)	21	23	24	23	QST leads
Wafer Yield (%)	94.2	~88 (est.)	~82 (est.)	~85 (est.)	QST significantly ahead
Gate Delay (ps)	5.8	6.1	6.4	6.0	QST leads
Power (relative)	1.00×	1.05×	1.12×	1.03×	QST baseline
ASP ($/wafer)	$16,800	$16,500	$14,000	N/A (internal)	QST premium pricing

Appendix G: Information Security Assessment

Assessment conducted by: Colonel (Ret.) James D. Hayes, VP Security & Compliance **Date**: February 2026 **Classification**: TOP SECRET

Physical Security

Layer	Measure	Status
Perimeter	Fence, CCTV (142 cameras), 24/7 security patrol	✅ Active
Building Access	Badge + PIN, biometric (fingerprint) for cleanroom	✅ Active
Cleanroom Access	Badge + PIN + biometric + mantrap	✅ Active
Server Room (Bldg C, Rm 112)	Badge + PIN + biometric + retinal scan	✅ Active
Visitor Escort	Mandatory for all non-badged personnel	✅ Active
Background Checks	All employees, 7-year history	✅ Active
TS/SCI Clearance	12 employees, DoD adjudicated	✅ Active

Cybersecurity

System	Protection	Classification
Process Recipe Database	Air-gapped, encrypted at rest (AES-256), biometric access	Level 5
GitLab (Source Code)	On-premises, MFA, IP-whitelisted, encrypted	Level 4
Email & Collaboration	Microsoft 365 Government (GCC High)	Level 3
Financial Systems	NetSuite, SSO + MFA, role-based access	Level 3
Manufacturing Execution	Custom MES, network-segmented, no internet access	Level 4
Physical Access Logs	Retained 7 years, tamper-evident storage	Level 3

Penetration Test: Last conducted December 2025 by CrowdStrike. No critical or high-severity findings. 3 medium findings (all remediated). Next test scheduled June 2026.
Incident History: Zero data breaches in company history (2018-present). One attempted phishing attack (Q2 2025) — blocked by email gateway, no compromise.

Appendix H: Legal Matters

Pending Litigation

Case	Court	Filed	Status	Exposure
QST v. NanoEtch Inc. (patent infringement)	N.D. Cal	Sep 2024	Discovery phase	$45M (claimed damages)
Former employee [redacted]	Santa Clara Superior	Mar 2025	Settled (confidential)	$0 (settled)

Regulatory Filings

Filing	Agency	Date	Status
EPA TRI Report (Toxics Release Inventory)	EPA	Annual	Filed, compliant
Cal EPA DTSC Hazardous Waste	Cal EPA	Quarterly	Current
OSHA 300 Log	OSHA	Annual	Filed, 1 minor injury FY2025
ITAR Registration	DDTC	Annual	Active, registration code M-12847
ECCN Classification (3 items)	BIS (Commerce)	Pending	Under review, estimated Q2 2026
FCC Equipment Authorization	FCC	As needed	Current for all applicable products

Insurance Coverage

Policy	Carrier	Coverage	Annual Premium
General Liability	AIG	$50M	$420K
Directors & Officers (D&O)	Chubb	$25M	$180K
Cyber Liability	Beazley	$15M	$95K
Property & Equipment	Zurich	$2.0B (replacement)	$1.2M
Key Person (Townsend, Tanaka)	MetLife	$50M combined	$340K
Product Liability	Liberty Mutual	$25M	$280K

Appendix I: Acquisition Structure Recommendations

Valuation Summary

Method	Enterprise Value	EV/Revenue	EV/EBITDA
DCF (Base Case, 10yr)	$5.1B	6.0×	21.3×
DCF (Upside Case)	$6.2B	7.3×	25.8×
DCF (Downside Case)	$3.8B	4.5×	15.8×
Comparable Transactions	$4.8B	5.7×	20.0×

Comparable Public Companies	$5.3B	6.3×	22.1×
Recommended Range	**$4.2B - $5.8B**	**5.0× - 6.8×**	**17.5× - 24.2×**

Key Deal Terms to Negotiate

Term	Recommendation	Rationale
Earnout	15-20% of purchase price tied to Apple renewal	De-risks key customer concentration
Management Retention	$45M pool for top 20 executives	Retain Townsend, Tanaka, key engineers
Non-Compete	3 years for Townsend, Tanaka	Protect competitive advantage
IP Escrow	All Level 5 [redacted] in escrow	Ensure continuity if key personnel depart
Working Capital	Peg at $180M	Standard mechanism
Indemnification	10% cap, 18-month survival	Market standard
CFIUS Condition	Closing conditioned on CFIUS clearance	Regulatory requirement

Financing Structure (Recommended)

Component	Amount	Source	Terms
Equity (Fund)	$2.0B	Meridian Capital Fund VIII	LP commitment
Senior Secured Debt	$1.5B	Goldman Sachs / JPMorgan	SOFR + 275bps, 5yr
Mezzanine	$0.5B	Ares Management	PIK toggle, 10.5%
Seller Notes	$0.3B	Townsend / Tanaka	3yr, 5.0%
Total	**$4.3B**		

Appendix J: Key Contacts

QST Management

Name	Title	Phone	Email	Address
Richard P. Townsend	CEO	(510) 555-0192	rtownsend@qst-semi.com	1847 Hillview Terrace, Los Altos, CA 94024
Dr. Yuki Tanaka	CTO	(510)	ytanaka@qst-	920 Oak Creek Drive, Palo

		555-0234	semi.com	Alto, CA 94301
Michael S. Brennan	CFO	(510) 555-0178	mbrennan@qst-semi.com	3340 Vineyard Ave, Pleasanton, CA 94566
Dr. Priya Venkatesh	VP Engineering	(510) 555-0256	pvenkatesh@qst-semi.com	560 Fremont Blvd, Fremont, CA 94538
Lisa M. Chow	VP Business Dev	(510) 555-0189	lchow@qst-semi.com	2100 University Ave, Palo Alto, CA 94301
Col. (Ret.) J.D. Hayes	VP Security	(510) 555-0201	jhayes@qst-semi.com	890 Mission Blvd, Fremont, CA 94539

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Firm	Contact	Role	Phone	Email
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Goldman Sachs	Robert Chen	Financing	(212) 555-0234	rchen@gs.com
Deloitte	Amanda Foster	Financial DD	(415) 555-0189	afoster@deloitte.com
Ocean Tomo	Dr. James Malackowski	IP Valuation	(312) 555-0167	jmalackowski@oceantomo.com

Key Suppliers

Company	Contact	Role	Phone	Email
ASML	Pieter de Groot	Account Mgr	+31-40-268-3804	p.degroot@asml.com
Lam Research	Jennifer Walsh	Strategic Acct Dir	(510) 555-0289	jwalsh@lamresearch.com
Applied Materials	Kevin Park	Key Acct Mgr	(408) 555-0312	kpark@amat.com
KLA Corporation	Dr. Chen Wei	Technology Dir	(408) 555-0197	cwei@kla.com
Toyo Gosei	Hiroshi Yamada	Sales Dir	+81-43-255-5801	hyamada@toyogosei.co.jp
Shin-Etsu	Takeshi Suzuki	Acct Mgr	+81-3-3242-4151	tsuzuki@shinetsu.co.jp

Appendix K: Glossary

Abbreviation	Full Term
ALD	Atomic Layer Deposition
APC	Advanced Process Control
BEOL	Back-End-Of-Line
BIS	Bureau of Industry and Security (US Dept. of Commerce)
CalEPA	California Environmental Protection Agency
CD	Critical Dimension
CD-SEM	Critical Dimension Scanning Electron Microscope
CFIUS	Committee on Foreign Investment in the United States
CMP	Chemical Mechanical Planarization
COGS	Cost of Goods Sold
Cpk	Process Capability Index
Cu	Copper
CVD	Chemical Vapor Deposition
DIBL	Drain-Induced Barrier Lowering
DDTC	Directorate of Defense Trade Controls

DUV	Deep Ultraviolet (lithography)
EBITDA	Earnings Before Interest, Taxes, Depreciation & Amortization
ECCN	Export Control Classification Number
EM	Electromigration
EOT	Equivalent Oxide Thickness
EPA	Environmental Protection Agency
EUV	Extreme Ultraviolet (lithography)
FEOL	Front-End-Of-Line
FO4	Fan-Out 4 (inverter delay metric)
GAA	Gate-All-Around (transistor architecture)
GCC High	Government Community Cloud High (Microsoft)
HfO_2	Hafnium Oxide
HSR Act	Hart-Scott-Rodino Antitrust Improvements Act
HTOL	High Temperature Operating Life (reliability test)
HCI	Hot Carrier Injection
ITAR	International Traffic in Arms Regulations
LTSA	Long-Term Supply Agreement
MFA	Multi-Factor Authentication
MSA	Master Supply Agreement
MTr	Million Transistors
NBTI	Negative Bias Temperature Instability
OES	Optical Emission Spectroscopy
OSHA	Occupational Safety and Health Administration
PAG	Photoacid Generator
PE-ALD	Plasma-Enhanced Atomic Layer Deposition
PGMEA	Propylene Glycol Monomethyl Ether Acetate
PVD	Physical Vapor Deposition

QST	Quantum Semiconductor Technologies, Inc.
R&D	Research & Development
RCE	Request for Continued Examination (patent prosecution)
SADP	Self-Aligned Double Patterning
SAQP	Self-Aligned Quadruple Patterning
SG&A	Selling, General & Administrative
SRAM	Static Random-Access Memory
STI	Shallow Trench Isolation
TDDB	Time-Dependent Dielectric Breakdown
TEMAH	Tetrakis(ethylmethylamido)hafnium
TiN	Titanium Nitride
TaN	Tantalum Nitride
TS/SCI	Top Secret / Sensitive Compartmented Information
WAT	Wafer Acceptance Test
WPH	Wafers Per Hour

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Signatures

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Date: March 15, 2026

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Date: March 15, 2026

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END OF REPORT

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